

## Claims

What is claimed is:

- 1           1.     A method for implementing power control in multi-voltage  
2 input/output (I/O) circuits comprising the steps of:  
3           providing first current biasing devices for creating a first constant bias  
4 current;  
5           providing second current biasing devices for creating a second bias  
6 current; and  
7           activating said second current biasing devices at a first voltage; and  
8 deactivating said second current biasing devices at a second voltage; said  
9 first voltage being less than said second voltage.
- 1           2.     A method for implementing power control as recited in claim 1  
2 wherein the step of providing said first current biasing devices for creating  
3 said first constant bias current includes the steps of constantly activating  
4 said first current biasing devices at both said first voltage and said second  
5 voltage.
- 1           3.     A method for implementing power control as recited in claim 1  
2 wherein the step of providing said second current biasing devices for  
3 creating said second bias current includes the steps of providing said second  
4 current biasing devices in parallel with said first current biasing devices; and  
5 applying a control input to said second current biasing devices for selectively  
6 activating said second current biasing devices at said first voltage; and  
7 deactivating said second current biasing devices at said second voltage.
- 1           4.     A method for implementing power control as recited in claim 1  
2 wherein each of the steps of providing said first current biasing devices and  
3 providing said second current biasing devices includes the steps of providing  
4 a plurality of field effect transistors (FETs).
- 1           5.     A method for implementing power control as recited in claim 4  
2 includes the steps of providing respective field effect transistors (FETs) of  
3 said second current biasing devices in parallel with respective field effect  
4 transistors (FETs) of said first current biasing devices.

1           6.     A method for implementing power control as recited in claim 5  
2 includes the steps of connecting a gate input of respective field effect  
3 transistors (FETs) of said first current biasing devices to a gate input of  
4 respective field effect transistors (FETs) of said second current biasing  
5 devices at said first voltage and disconnecting said gate inputs of respective  
6 field effect transistors (FETs) of said second current biasing devices at said  
7 second voltage.

1           7.     A method for implementing power control as recited in claim 1  
2 wherein the steps of activating said second current biasing devices at a first  
3 voltage; and deactivating said second current biasing devices at a second  
4 voltage includes the steps of providing a bias control generating circuit  
5 coupled to said second current biasing devices for activating said second  
6 current biasing devices at said first voltage; and deactivating said second  
7 current biasing devices at said second voltage.

1           8.     A method for implementing power control as recited in claim 1  
2 wherein the steps of activating said second current biasing devices at a first  
3 voltage; and deactivating said second current biasing devices at a second  
4 voltage includes the steps of providing a bias control generating circuit for  
5 generating a control input for activating said second current biasing devices  
6 at said first voltage; and generating said control input for deactivating said  
7 second current biasing devices at said second voltage.

1           9.     A method for implementing power control as recited in claim 8  
2 wherein said control input includes a gate input applied to respective field  
3 effect transistors (FETs) of said second current biasing devices.

- 1           10.   Apparatus for implementing power control in multi-voltage  
2 input/output (I/O) circuits comprising:  
3           a first set of current biasing devices for creating a first constant bias  
4 current;  
5           a second set of current biasing devices for creating a second bias  
6 current; and  
7           a control input for activating said second set of current biasing  
8 devices at a first voltage; and for deactivating said second set of current  
9 biasing devices at a second voltage; said first voltage being less than said  
10 second voltage.
- 1           11.   Apparatus for implementing power control as recited in claim  
2 10 includes a bias control generating circuit for generating said control input.
- 1           12.   Apparatus for implementing power control as recited in claim  
2 10 wherein each of said first set of said current biasing devices and said  
3 second set of said current biasing devices includes a plurality of field effect  
4 transistors (FETs).
- 1           13.   Apparatus for implementing power control as recited in claim  
2 12 wherein said plurality of field effect transistors (FETs) of said first set of  
3 said current biasing devices are constantly activated and controlled by a  
4 constant gate input.
- 1           14.   Apparatus for implementing power control as recited in claim  
2 12 wherein said plurality of field effect transistors (FETs) of said second set  
3 of said current biasing devices are selectively activated at said first voltage  
4 and controlled by a switched gate input.
- 1           15.   Apparatus for implementing power control as recited in claim  
2 14 wherein said plurality of field effect transistors (FETs) of said second set  
3 of said current biasing devices are coupled to a bias control generating  
4 circuit providing said switched gate input and selectively activated at said  
5 first voltage.